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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,495	09/26/2003	Lawrence W. Golick	2	3528

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/672,495	GOLICK, LAWRENCE W.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/25/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4-8 and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (US 6121690), hereinafter Yamada in view of Yuan et al. (US 6713850), hereinafter Yuan.

Regarding claims 1 and 15, Fig. 4 of Yamada shows a packaged integrated circuit comprising:

a die (1; an IC);

a package body formed from encapsulant, at least partially enclosing the die (shown in Fig. 2);

a leadframe connected to the die and at least partially enclosed within the package body, and having leads (6) extending from the package body, a subset of the leads of the leadframe being separated by a lead-to-lead pitch, wherein at least two adjacent leads of the leadframe are separated by a space larger than the pitch (shown along the center line 5).

Yamada shows the most aspect of the instant invention except "at least one additional lead connected to the die and disposed on an underside of the package body, the at least one additional lead being connectable to a circuit mounting structure trace passing between the adjacent leads separated by the space larger than the pitch."

Fig. 2B of Yuan shows a semiconductor device with at least one additional lead (232; a dummy lead with a dummy pad) connected to the die and disposed on an underside of the package body (col. 3, line 65 – col. 3, line 4) and the at least one additional lead being connectable to a circuit mounting structure (through being electrically conductive) while passing between the adjacent leads separated by the space larger than the pitch.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yuan into the device of Yamada in order to have "at least one additional lead connected to the die and disposed on an underside of the package body, the at least one additional lead being connectable to a circuit mounting structure trace passing between the adjacent leads separated by the space larger than the pitch" for a better support.

Regarding claim 4, Fig. 2B of Yuan shows a semiconductor device wherein the at lest one additional lead is disposed adjacent to die on the underside of the package.

Regarding claims 5 and 6, Fig. 2B of Yuan shows the at least one additional lead is disposed on each side of the die on the underside of the package body closest to the space larger than the pitch.

Regarding claim 7, Fig. 2B of Yuan shows a space larger than the pitch is disposed between two adjacent leads on each side of the package body.

Regarding claim 8, Fig. 4 of Yamada shows the packaged integrated circuit is configured as a Thin Quad Flat Package, TQFP (col. 4, line 19).

Regarding claim 10, Fig. 2B of Yuan shows the leads (I/O functional lead; col. 4, line 48) in the subset of leads separated by the lead-to-lead pitch of the leadframe are configured for carrying data and control signals.

Regarding claim 11, the combined teachings of Yamada and Yuan fail to show "the at least one additional lead is configured for carrying a signal having a frequency of at least 2 GHz." However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have at least one additional lead configured for carrying a signal having a frequency of at least 2 GHz for a high speed application since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 12, the combined teachings of Yamada and Yuan fail to show "the lead-to-lead pitch is approximately 0.4 mm wide." However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the lead-to-lead pitch approximately 0.4 mm wide in order to accommodate a design specification since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 13, the combined teachings of Yamada and Yuan fail to show "each lead of the leadframe is approximately 0.2 mm wide." However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have each lead of the leadframe approximately 0.2 mm wide in order to accommodate a design specification since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 14, the combined teachings of Yamada and Yuan fail to show "the space larger than the pitch is determined by the equation, $LP = wx + p(x+1)$, wherein LP represents the space larger than pitch, w represents a width of the leadframe leads, p represents the lead-to-lead

pitch, and x represents the number of leadframe leads removed to form the space larger than pitch." However, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the space larger than the pitch determined by the equation, LP = wx + p(x+1) in order to accommodate a design specification since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch,* 617 F.2d 272, 205 USPQ 215 (CCPA 1980). It is known in the art that lead spacing can be determined through adjustment of a width of the lead frame and lead pitch.

Claims 2, 3, 9, 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada and Yuan as applied to claim 1 above, and further in view of Hayashida et al.(US 6060768), hereinafter Hayashida.

Regarding claim 2, the combined teachings of Yamada and Yuan shows most aspect of the instant invention except "the at least one additional lead is wire bonded to the die within the package body." Fig. 1 of Hayashida shows a lead (3) on the semiconductor device is wire-bonded (8) to the die within the package body.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hayashida into the device of Yamada and Yuan in order to have "the at least one additional lead is wire bonded to the die within the package body" to have a lead on chip configuration.

Regarding claim 3, the combined teachings of Yamada and Yuan shows most aspect of the instant invention except "the at least one additional lead is substantially flush with the

underside of the package body." Fig. 28 of Hayashida shows a lead (3) is substantially flush with the underside of the package body (4).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hayashida into the device of Yamada and Yuan in order to have "the at least one additional lead is substantially flush with the underside of the package body" to minimize the package dimension.

Regarding claim 9, the combined teachings of Yamada and Yuan show most aspect of the instant invention except "a die pad of the die is exposed on the underside of the packaged integrated circuit." Fig. 28 of Hayashida shows a die pad of the die is exposed on the underside of the packaged integrated circuit.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hayashida into the device of Yamada and Yuan in order to have "a die pad of the die is exposed on the underside of the packaged integrated circuit." " to connect the external circuitry.

Regarding claim 16, Fig. 4 of Yamada shows a packaged integrated circuit comprising:

a die (1; an IC);

a package body formed from encapsulant, at least partially enclosing the die (shown in Fig. 2);

a leadframe connected to the die and at least partially enclosed within the package body, and having leads (6) extending from the package body, a subset of the leads of the leadframe being separated by a lead-to-lead pitch, wherein at least two adjacent leads of the leadframe are separated by a space larger than the pitch (shown along the center line 5).

Yamada shows the most aspect of the instant invention except "at least one additional lead connected to the die and disposed on an underside of the package body, the at least one additional lead being connectable to a circuit mounting structure trace passing between the adjacent leads separated by the space larger than the pitch."

Fig. 2B of Yuan shows a semiconductor device with at least one additional lead (232; a dummy lead with a dummy pad) connected to the die and disposed on an underside of the package body (col. 3, line 65 – col. 3, line 4) and the at least one additional lead being connectable to a circuit mounting structure (through being electrically conductive) while passing between the adjacent leads separated by the space larger than the pitch.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yuan into the device of Yamada in order to have at least one additional lead connected to the die and disposed on an underside of the package body, the at least one additional lead being connectable to a circuit mounting structure trace passing between the adjacent leads separated by the space larger than the pitch" for a better support.

The combined teachings of Yamada and Yuan show most aspect of the instant invention except "so that the trace is connectable to an additional lead on an underside of the package body." Fig. 28 of Hayashida shows the lead on an underside of the package body is contactable to the circuitry.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hayashida into the device of Yamada and Yuan in order to have "so that the trace is connectable to an additional lead on an underside of the package body" to connect the external circuitry.

Regarding claim 20, Fig. 4 of Yamada shows a packaged integrated circuit comprising:

a die (1; an IC);

a package body formed from encapsulant, at least partially enclosing the die (shown in Fig. 2);

a leadframe connected to the die and at least partially enclosed within the package body, and having leads (6) extending from the package body, a subset of the leads of the leadframe being separated by a lead-to-lead pitch, wherein at least two adjacent leads of the leadframe are separated by a space larger than the pitch (shown along the center line 5).

Yamada shows the most aspect of the instant invention except "at least one additional lead connected to the die and disposed on an underside of the package body, the at least one additional lead being connectable to a circuit mounting structure trace passing between the adjacent leads separated by the space larger than the pitch."

Fig. 2B of Yuan shows a semiconductor device with at least one additional lead (232; a dummy lead with a dummy pad) connected to the die and disposed on an underside of the package body (col. 3, line 65 – col. 3, line 4) and the at least one additional lead being connectable to a circuit mounting structure (through being electrically conductive) while passing between the adjacent leads separated by the space larger than the pitch.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yuan into the device of Yamada in order to have at least one additional lead connected to the die and disposed on an underside of the package body, the at least one additional lead being connectable to a circuit mounting structure trace passing between the adjacent leads separated by the space larger than the pitch" for a better support.

The combined teachings of Yamada and Yuan show most aspect of the instant invention except "at least one additional lead connected to the die and disposed on an underside of the package body, the at least one additional lead being connectable to a trace of the circuit mounting structure routed from the at least one electrical connector and passing between the adjacent leads separated by the space larger than the pitch."

Fig. 28 of Hayashida shows the lead on an underside of the package body is contactable to the circuitry. And Fig. 28 of Hayashida shows the exposed lead connecting to the board, therefore routing the signal from an electrical connector, and passing to the bond pad (6) which is connected to the exposed lead.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Hayashida into the device of Yamada and Yuan in order to have "so that the trace is connectable to an additional lead on an underside of the package body" to connect the external circuitry.

Regarding a limitation in the preamble, Fig. 1 of Hayashida shows a circuit mounting structure (10) comprising at least one electrical connector (9), a plurality of traces, and at least one packaged integrated circuit (2) mounted thereon.

Claims 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada, Yuan and Hayashida as applied to claim 16 above, and further in view of Yee et al. (US 64448633), hereinafter Yee.

Regarding claim 17, the combined teachings of Yamada, Yuan and Hayashida show most aspect of the instant invention except "at least one locking mechanism coupled between the

adjacent leads having the space larger than the pitch therebetween, the locking mechanism being configured to maintain the space larger than the pitch." Fig. 3A of Yee shows a lead frame with a locking mechanism (14) between the adjacent leads.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yee into the device of Yamada, Yuan and Hayashida in order to have "at least one locking mechanism coupled between the adjacent leads having the space larger than the pitch therebetween, the locking mechanism being configured to maintain the space larger than the pitch." to ensure a stable layout of the lead frame.

Regarding claim 18, the combined teachings of Yamada, Yuan and Hayashida show most aspect of the instant invention except "the locking mechanism is at least partially enclosed within the package body." Fig. 5E of Yee shows a lead frame with a locking mechanism (14) between the adjacent leads.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yee into the device of Yamada, Yuan and Hayashida in order to have a locking system enclosed within the packaging body to protect the locking mechanism.

Regarding claim 19, the combined teachings of Yamada, Yuan and Hayashida show most aspect of the instant invention except "the locking mechanism is U-shaped having a central portion arranged within the package body and first and second legs each extending toward a perimeter of the package body when the leadframe is used in a packaged integrated circuit.." Fig. 5D-1 (or Fig. 6B) of Yee shows a lead frame with a U-shaped locking mechanism (14), each leg extending toward a perimeter of the package body. It would have been obvious to one of

ordinary skill in the art at the time of the invention was made to incorporate the teachings of Yee into the device of Yamada, Yuan and Hayashida in order to have a locking system U-shaped locking mechanism (14), each leg extending toward a perimeter of the package body to prevent the separation of the inner leads.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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